REMARKS/ARGUMENTS

Claims 1-2, 6, 7, 10, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al. (US 5,648,662). Claims 12-13, 16, 18, 20-21, 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (US 5,365,080). Claims 1-7 and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harkin et al. (U.S. 5,705,413). Claims 10-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harkin et al. (U.S. 5,705,413) in view of Kawasaki et al. (U.S. 6,426,245).

1. Correction of claim 23:

Claim 23 is amended because there is a typo in claim 23. The term "heat-retain" is replaced by the term "heat-retaining". Acceptance of the amended claim 23 is politely requested.

2. Rejection of claims 1-2, 6, 7, 10, 23-24:

Claims 1-2, 6, 7, 10, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al. (US 5,648,662) for reasons of record, as recited on pages 2-4 of the above-indicated Office action.

Response:

(1) Claim 1:

According to claim 1 of the present application, the method comprises forming a buffer layer 112 on a substrate, *forming an amorphous silicon film 114 on the buffer layer 112, and forming a mask layer 116 on the amorphous silicon film 114.* Then, a photo-etching process is performed to remove a portion of the mask layer 116 in the first region 120 to expose the amorphous silicon film 114 in the first region 120, while the mask layer 116 in the second region 130 remains on the amorphous silicon film 114 and *the overall amorphous silicon film 114 are intact.* Then, a CVD process is performed to form a heat-retaining capping layer 118 covering the mask layer 116 in the second region 130 and the exposed amorphous silicon film 114. An excimer laser crystallization process is then performed to complete melt and re-crystallize the

amorphous silicon film 114, in the first region 120; meanwhile, *the amorphous silicon film 114, in the second region 130, is only partially melted or not completely melted because it is covered by the mask layer 116*. Therefore, when excimer laser process is stopped for re-crystallizing the amorphous silicon film 114 in the first region 120, the crystallization will start at the boundary between the first region and the second of the amorphous silicon film 114 to gain preferable crystal quality. From the above-description, the method of the present application keeps the mask layer 116 in the second region 130 to cover the amorphous silicon film 114, and all the heat-retaining capping layer 118, the mask layer 116, and the amorphous silicon film 114 in the second region 130 will be removed together to form a polysilicon island.

The characteristics of the present application include utilizing the heat-retaining capping layer 118 covering the first region 120 to reduce the heat dissipation rate so that the amorphous silicon film 114 right under and directly contacting the heat-retaining capping layer 118 can be maintained in a higher temperature environment for a longer time to perform the crystallization, leading to increase the grain size effectively resulted in better crystallization quality (para [0019]).

According to the specification and Fig.1 and Fig.3A-3H of the application of Zhang et al., they disclose forming a base film 2 on a glass substrate 1 to prevent intrusion of impurities from the substrate (col.3, lines 6-8), performing a first etching process to form a gate 3. After removing the photomask layer P1, a gate insulating film (SiN_X) 4 is formed. Then, an intrinsic amorphous silicon film 5 and a doped amorphous silicon layer 6 are formed on the substrate entirely. *A second etching process is following performed by using a second photomask P2 to form a* ***TFT island.*** *After removing the second photomask P2, a third photomask P3 is formed to perform a third etching process to form source/drain.* The third photomask P3 is removed. A passivation film (cap layer) 13 is then formed to protect the whole TFT device to prevent disturbance of the upper surface of the amorphous silicon film 5 due to a laser irradiation. After that, Laser radiation was illuminated from above the device. (col.2, lines 60 to col.3, lines 26, and col.7, lines 17-27).

The Examiner points that the passivation film 13 of Zhang et al. is the heat-retaining capping layer of the present application in the above-identified Office Action. However, *Zhang et al describes clearly that the passivation film 13 is only used to prevent disturbance of the upper surface of the film when it is irradiated with the laser radiation (Col.2, line 60 to col.3, line 3) and never mention that the passivation film 13 may have the heat-regaining function to lower heat dissipation rate nor suggest utilizing the passivation film 13 to providing a higher temperature to the amorphous silicon film 5 that contacts the passivation film 13 during the crystallization process for increasing the crystal grain size and crystal quality.* Therefore, applicant respectfully believes that it is not appropriate to consider the passivation film 13 of Zhang et al. as the heat-retaining capper in claim 1 of the present application. Even when the passivation film 13 is silicon oxide that may be one of the materials of the heat-retaining capping layer, the passivation film 13 should not be regarded as the heat-retaining capping layer. Accordingly, applicant contends that Zhang et al. never disclose utilizing a heat-retaining capping layer.

In addition, Zhang et al. teach *performing an etching process to each the amorphous film 5 and the doped amorphous film 6 to form a TFT island in the active area at first, forming the passivation layer 13, and then performing a laser process to crystallize the amorphous film 5*. In contrast, the present application method forms the amorphous film completely on the substrate, utilizes the mask layer to define the crystallization region, the first region, without etching the amorphous silicon film, and perform the excimer layer process to re-crystallize the amorphous silicon film for forming polysilicon film in the first region. After that, the mask layer and heat-retaining capping layer are removed, and then the polysilicon layer is etched to form the active area. In other words, *the present application forms the polyslicon film first by the excimer laser and then performs the etching process to remove the amorphous silicon film in the second region and leave the polyslicon film in the first region*. Compare the flat polysilicon film 122 (or the amorphous silicon layer 114, 214) in Figs.4-8 of the present application with Figs. 1(a), 1(b), 3(A)-3(H) of Zhang et al., which has a patterned non-conformal amorphous silicon film 5 covering the gate insulator 4 of the application of Zhang et al., one could see the above-mentioned

differences of the fabrication process sequences between the present application and the prior art.

Furthermore, *the Zhang et al. disclose clearly that the laser radiation having a sufficient energy is irradiated to crystallize the whole intrinsic amorphous silicon layer 5, even those portions of which are under the source region 11, the drain region 12, the source electrode 9, and the drain electrode 10. Therefore, the whole amorphous silicon film 5 becomes a polysilicon film to serve as the channel formation region 5* (col.2, lines 37-49). Accordingly, *the source and drain electrodes 9, 10 or the source and drain region 11, 12 cannot serve as a mask layer blocking the laser radiation in claim 1 of the present application.*

In contrast, the mask layer defined in claim 1 of the present application can increase the reflection rate to reduce the heat absorption of the amorphous silicon film or increase the thermal conductivity to increase the heat dissipation of the amorphous silicon film to form a heterogeneous interface between the amorphous silicon film covered and not covered by the mask layer.

In conclude, the differences between the present application and Zhang et al. are listed as following:

(1) The present application performs the excimer laser process to re-crystallize the amorphous silicon film for forming the polysilicon film before etching the silicon film in the second region. However, Zhang et al. first form the TFT island (etch the amorphous silicon film) and then use laser to crystallize the amorphous silicon. The fabrication methods are obviously different.

(2) Zhang et al. never mention to use heat-retaining capping layer covering the amorphous silicon film for reducing heat dissipation rate to provide a high temperature environment in a longer time to re-crystallize the silicon film and to effectively improve the crystal gain sizes.

(3) Zhang et al. is silent about forming a mask layer on the amorphous silicon film to block laser irradiation to for keep a low temperature for the amorphous silicon

film right below the mask layer. In the present application, the mask layer blocks laser irradiation, resulted in the amorphous silicon film covered by the mask layer not melted and a heterogeneous interface occurring, which leads the grown direction of the crystal grains in the first region (para. [0019], lines 4-7).

Therefore, applicant believes claim 1 is quite different from Zhang et al. and Zhang et al. do not disclose all the limitations in claim 1. Applicant thus alleges the rejection of claim 1 under 102(b) should not be valid. Reconsideration of claim 1 is politely requested.

(2) Claims 2, 6, 7, 10, 23-24:

Similar to the above discussion, Zhang et al. do not disclose all the limitations in claims 6, 7, 10, and 24 respectively. For example, *Zhang et al. do not teach forming a heat-retaining capping layer and which comprises a silicon nitride layer, a metal layer, or a silicon-oxy nitride in claim 7.* Zhang et al. do not disclose that the excimer laser comprises a long duration laser in claim 10, neither. *Zhang et al. do not teach a mask layer comprising a multi-layer structure and all the layers of the mask layer have the function to block laser irradiation,* which is described in claim 6. Furthermore, *Zhang et al. never mention or suggest to form a heat-retaining capping layer that reduces the heat dissipation rate in the crystallization process and maintains the amorphous silicon film in the first region in a higher temperature environment when performing the excimer laser crystallization for increasing grain sizes of the polysilicon film effectively,* which is defined in claim 24 and para [0019] of the present application. Therefore, applicant believes claims 6, 7, 10, and 24 should be allowable. In addition, claims 2 and 23 are dependent upon claim 1, and they should be allowable if claim 1 is allowable. Reconsideration of claims 2, 6, 7, 10, 23-24 is politely requested.

(3) Claims 3-5, 8-9, 11:

The Examiner never mentions that claims 3-5, 8-9, 11 are anticipated by Zhang et al. Regarding to claim 3, it defines that the heat-retaining capping layer, the mask layer, and the amorphous silicon film in the second region are etched and removed

after forming the polysilicon film by the excimer laser. However, *Zhang et al. never disclose performing an etching process to remove a heat-retaining capping layer, the passivation film 13 (in Fig.1(a)), a mask layer, an amorphous silicon film or a polysilicon film in the second region after the exicmer laser crystallization process.* A person having ordinary skill in the art can easily distinguish the differences of the method and structure between Zhang et al. and the present application because there is no heat-retaining capping layer, mask layer and amorphous silicon film existing after the laser crystallization.

Regarding to claim 5, Zhang et al. are also silent about that the mask layer comprises a silicon oxide layer, a silicon nitride layer, or a silicon-oxy nitride layer.

Regarding to claims 8-9, Zhang et al. never mention the laser make amorphous silicon film in the second region covered by the mask layer become partially melted and make the amorphous film in the first region become completely melted so that grains are grown laterally toward the first region from the interface between the first region and the second region to form a polysilicon film in the first region. Zhang et al. do not mention the heat-retaining capping layer is used to decrease the heat dissipating rate of the amorphous silicon film for increasing the size of the grains formed in the excimer laser crystallization process.

Regarding to claim 11, Zhang et al. do not teach using a long duration laser having a period in a range of about 150 to 250 ns, either.

Accordingly, *in comparison with the application of Zhang et al., claims 3-5, 8-9, 11 should be allowable and are allowable subject matters.*

3. Rejection of claims 12-13, 16, 18, 20-21, 25-26:

Claims 12-13, 16, 18, 20-21, 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (US 5,365,080) for reasons of record, as recited in pages 3-4 of the above-identified Office Action.

Response:

(1) Claim 12:

According to claim 12 of the present application, the method comprises forming an amorphous silicon film on a substrate, forming a heat-retaining capping layer covering the amorphous silicon film, forming a patterned mask layer on the heat-retaining capping layer and the amorphous silicon film in the first region, and performing a excimer layer crystallization process to make the amorphous silicon film in the first region crystallize to a polysilicon film.

Regarding to the application of Yamazaki et al., their method includes forming a coating 402 on a portion of the substrate 401, changing (crystallizing) the surface structure of the coating 402 into either polycrystals or a single crystal 402a by laser annealing or other similar method, and forming a thin insulating film on the polycrystals 402a. (Fig.4(C), col.3, lines 64 to col.4, lines 5). Then, a gate 406 is formed on the thin insulating film. The gate 406 is next used as a mask to perform an ion implantation process to form source/drain 403, 404, 408, 409. A crystallization process is again performed to change the structure semiconductor coating 402a and the underlying semiconductor layer 402 (Figs.4(D), 4(E)). Accordingly, *Yamazaki et al. etch the semiconductor coating 402 to form a transistor island region, perform a first surface crystallization process to the surface of the coating 402, and performing a second crystallization process after forming the gate 406 on the coating 402, wherein Yamazaki et al. is silent about that the gate 406 blocks the laser to form a heterogeneous interface so as to control the grown direction of crystal grains. In addition, Yamazaki et al. never teach forming a heat-retaining layer on a first region to reduce the heat dissipation rate for providing a high temperature environment for the re-crystallization of the amorphous silicon film resulted in increasing the gain sizes.* Therefore, Yamazaki et al. disclose obvious different method and structure from the method and structure of the present application. Accordingly, applicant contends claim 12 should be allowable. Reconsideration of claim 12 is respectfully requested.

(2) Claims 13, 16, 18, 20-21, 25-26:

Regarding claim 13, *Yamazaki et al. do not disclose forming a* ***buffer layer*** *for*

prevent impure materials from diffusing upward in latter processes and affecting the quality of the polysilicon film (para. [0017], lines 6-8).

Regarding claim 16, Yamazaki et al. do not disclose all the limitations that the mask layer comprises a silicon oxide layer, a silicon nitride layer, a metal layer, or a silicon-oxy nitride layer in claim 16.

Regarding claims 18, 20, Yamazaki et al. never teach forming a heat-retaining capping layer that comprises a silicon oxide layer, a silicon nitride layer, or a silicon-oxy nitride layer and *never mention the heat-retaining capping layer is used to decrease heat dissipating rate of the amorphous silicon film for increasing the grain sizes.*

Yamazaki et al. are silent about forming a heat-retaining capping layer that can *provide a higher temperature environment under the laser crystallization for increasing grain sizes of the polysilicon film effectively* in claim 26 of the present application.

From the above-discussion, applicant believes claims 13, 16, 18, 20, 26 should be allowable. Furthermore, since claims 21 and 25 are dependent upon claim 12, they should be allowed if claim 12 is allowable. Reconsideration of claims 13, 16, 18, 20-21, 25-26 is hereby requested.

(3) Claims 14-15, 17, 19, and 22:

The Examiner never mentions that claims 14-15, 17, 19, and 22 are anticipated by Yamazaki et al. Regarding to claim 14, it defines that the mask layer, the heat-retaining capping layer, and the amorphous silicon film in the second region are etched and removed after forming the polysilicon film by the excimer laser. However, *Yamazaki et al. never disclose performing an etching process to remove a heat-retaining capping layer, a mask layer, an amorphous silicon film or a polysilicon film in the second region after the exicmer laser crystallization process.*

Regarding to claim 15, Yamazaki et al. never teach removing a heat-retaining capping layer by an etching process after forming the polysilicon film.

Regarding to claim 17, Yamazaki et al. are also silent about that the mask layer is a multi-layer structure.

Regarding to claims 19, Yamazaki et al. never mention the laser make amorphous silicon film in the second region covered by the mask layer become partially melted and make the amorphous film in the first region become completely melted so that grains are grown laterally toward the first region from the interface between the first region and the second region to form a polysilicon film in the first region.

Accordingly, *in comparison with the application of Yamazaki et al., claims 14-15, 17, 19, and 22 should be allowable and are allowable subject matters.*

4. Rejection of claims 1-7 and 12-18 under 35 U.S.C. 103(a):

Claims 1-7 and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harkin et al. (U.S. 5,705,413) for reasons of record, as recited in pages 4-5 in the Office Action.

Response:

According to claims 1 and 12 of the present application, when performing the excimer laser crystallization process, the amorphous silicon films 114, 214 in the first region 120, which are predetermined to be formed as polysilicon films, are *directly covered by the heat-retaining capping layers 118, 216*, as shown in Figs. 5 and 8. Therefore, *when performing the excimer laser crystallization process, the amorphous silicon film 114 is not directly exposed under the laser but is covered by the heat-retaining capping layer 118.* Since the heat-retaining capping layer 118 can reduce the heat dissipation rate in the crystallization process and maintain the amorphous silicon films 114, 214 in a higher temperature environment for more time, the present application has a obviously advantage that the fabricated polysilicon film

has increased grain size effectively (paragraph [0019], lines 7-12, paragraph 0023, lines 1-4).

According to Harkin's disclosure, a semiconductor film 1 is formed on an insulating substrate 10. Then a barrier insulating layer 20 and a masking pattern of thermally-stable absorbent or reflective inorganic material 21 is sequentially formed on the semiconductor film 1 (Fig. 3, 13, col. 6, lines 10-11, col. 7, lines 40-48, col. 12, lines 59-65). Before exposing the first portion 1a of the semiconductor film 1 to the energy beam, the barrier insulating layer 20'and the inorganic material 21' are removed from the first portion 1a of the semiconductor film 1 (Fig. 4-5, col. 6, lines 12-19, col. 7, lines 50-58, col. 12, lines 64-67, col. 13-14, lines 6-9). After that, the energy beam 25 is used to define the first and second portions 1a and 1b of different crystallinity (col. 6, lines 20-25, col.7, lines 61-63). Accordingly, *the un-masked first portion 1a of the semiconductor film 1 is directly exposed under the energy beam 25 during the crystallization process for crystallizing the un-masked first portion 1a of the semiconductor film 1 to become a polysilicon film* (col. 5, lines 60-64). Furthermore, the diffusion barrier 20 is against adverse effects of heat diffusion or impurity diffusion from the masking pattern of inorganic material (col. 3 lines 47-62), and the inorganic masking pattern 21 is stable with this laser beam and reflects the laser beam 25 from over the film portions 1b which are not to be crystallized (col. 7, lines 63-67, col. 8, lines 35-40). Thus, absolutely, *the Harkin's disclosure never teaches to use a heat-retaining capping layer to cover the amorphous film, which is predetermined to form a polysilicon film, for maintaining the semiconductor film in a higher temperature environment. On the other words, the amorphous film predetermined to form a polysilicon film of the Harkin's disclosure is directly exposed under the energy beam, but that of the present invention is covered by the* ***heat-retaining capping layer*** *under the energy beam so as to increase the grain size of the polysilicon film and improve the performance of devices.*

From the above discussion, the Applicant believes that the amended claims 1 and 12 of the present application are absolutely different from the Harkin's disclosure. Reconsideration of the amended claims 1 and 12 is therefore requested.

Furthermore, Harkin does not teach all the limitations in claims 2-7, 13-18. For example, Harkin is silent about forming a buffer layer on the substrate for prevent impure materials in the substrate from diffusing upward to the amorphous silicon film or the polysilicon film to affect the quality of the polysilicon film during the excimer laser process, and which is defined in claims 2, 13. Therefore they should be allowable. In addition, since claims 2-7 and 13-18 are dependent upon claim 1 and claim 12 respectively, they should be allowed if the amended claim 1 and claim 12 are allowed. Reconsideration of claims 2-7 and 13-18 is therefore requested.

5. Rejection of claims 10-11 and 21-22 under US.C. 103(a):

Claims 10-11 and 21-22 are rejected under 35 U.S.C 103(a) as being unpatentable over Harkin et al. (U.S. 5,705,413) in view of Kawasaki et al. (U.S 6,426,245), as cited in page 6 of the Office Action.

Response:

Claims 10-11 and 21-22 are dependent upon claim 1 and claim 12, and they should be allowed if claim 1 and claim 12 are allowed. Reconsideration of claims 10-11 and 21-22 is therefore requested.

6. Claims 8-9, and 18:

Examiner never mentions claims 8-9, and 18 are anticipated by any of the above-mentioned prior art. Therefore, they should be allowable subject matters. Allowance of claims 8-9 and 18 are hereby politely requested.

7. Double patenting:

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(C) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effectively January 1, 1994, a registered attorney or agent may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 12-19, 21-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-20 of copending Application No. 10/604,485. Although the conflicting claims are not identical, they are not patentably distinct from each other because '485 anticipated the claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response:

Without disclaimer as to the merits of the claims filed in this application, the applicant wishes to submit a terminal disclaimer in compliance with 37 CFR 1.321(c) as per the Examiner's suggestion. Also included with this response are the necessary documents to prove common ownership of the present application and the cited Patent. Acceptance of the terminal disclaimer is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: August 26, 2005

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